Techniques For Designing Testable Boards And Systems Based On Boundary-Scan Technology

Presented by Eric Cormack, DFT Consultant

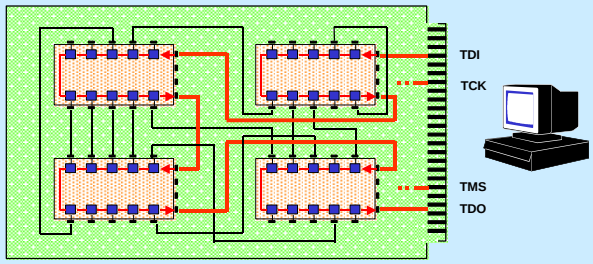
DURATION: 2 to 3 days

TARGET AUDIENCE digital board/system and field-service designers and test engineers, project managers, product support engineers.

MOTIVATION OBJECTIVES: to motivate chip and board designers to consider life-cycle test needs as an integral part of a product design process to the point where they proactively design in testability.

TEACHING OBJECTIVES: to identify the life-cycle needs of a product in respect of test; to present the basics of the IEEE 1149.1 Boundary Scan Standard; to identify the synergy of boundary scan, BIST and internal scan at system integration and field service levels of test using 1149.1 as a backplane test bus

Day 1
An introduction To The 1149.1 Boundary Scan Standard: Chip-Level Architecture and Board-Level Application, IEEE 1532 In-System Configuration Standard



Board-level Application of Boundary Scan: Interconnect Test

Day 1 is an introduction to the widely-accepted IEEE 1149.1-2001 Boundary Scan Standard and shows how boundary scan can be used to ease the prototype debug and volume manufacturing test of loaded printed-circuit board assemblies. The tutorial covers the basic chip-level architecture and Boundary-Scan Description Language (BSDL) but the emphasis will be on the use and benefits at board level, concentrating on pattern generation for detection and diagnosis of faults within the boundary scan domain. Handling faults outside the domain (cluster and memory-array tests) is also considered. Day 1 also includes an introduction to the IEEE 1532 In-System Configuration Standard leveraging 1149.1 structures to enable programming of CPLDs and FPGAs *in situ* on the board.

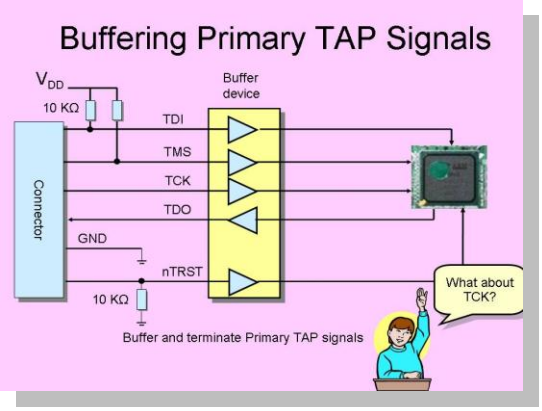
THE IEEE 1149.1-2001 TEST ACCESS PORT AND BOUNDARY-SCAN ARCHITECTURE STANDARD

- Motivation for boundary scan: use of surface mount packaging, double-sided multi-layer boards
- Device-level architecture: Test Access Port (TAP), Instruction Register, TAP controller, Bypass register, Identification register, Boundary-Scan register, access to internal registers
- Mandatory and optional public instructions: BYPASS, EXTEST, PRELOAD, SAMPLE, INTEST, IDCODE, USERCODE, CLAMP, HIGHZ, RUNBIST
- Conducting a "blind" interrogation
- Forms of boundary-scan cells: BC_1 to BC_10
- Using boundary scan at board level: board defects and fault models (opens and shorts: equivalent fault models)
- Scan path integrity test
- Interconnect test: generating patterns to detect and locate interconnect opens and shorts
- Languages and formats: Boundary Scan Description Language (BSDL)
- Handling the BS-to-nonBS interface: creating tests for RAM and non-RAM clusters
- Creating a board test program

IEEE 1532-2002 IN-SYSTEM CONFIGURATION STANDARD

- General architecture: system modal states
- *ISC_Enabled* and *ISC_Done* control signals
- Accessing the programmable memory array
- New mandatory and optional instructions
- ISC programming flow
- Extensions to BSDL: flows, procedures and actions

Day 2
Chip and Board DFT Guidelines, Board DFT Case Study, IEEE 1149.6 "AC-EXTEST" Standard for AC-Coupled LVDS Interconnects



Day 2 contains a comprehensive set of practical chip and board DFT guidelines, based on maximizing the use of on-board boundary-scan devices and introduces a systematic way of reviewing a board's testability, illustrated by a real-life case study. The special problem of dealing with configured or un-configured FPGAs is discussed in depth with relation to one of today's more complex FPGAs – the Xilinx Virtex-2 Pro and the more recent Virtex 4 and Virtex 5 devices.

The IEEE 1149.6 "AC-EXTEST" Standard, applied to the testing of high-speed AC-coupled low-voltage differential signal buses, is also discussed, together with other ways of testing High-Speed Serial IO buses such as loopback test and the use of Interconnect BIST engines (IBIST).

BOARD DFT BASED ON BOUNDARY SCAN

- Chip-level DFT guidelines, including:
  - Adding extra 1149.1 features inside the chip
  - Verifying BSDL compliance and validating the BSDL files
  - Increasing coverage by replacing BC_1s with BC_7s
  - Reduced Pin-Count Test
- Board level DFT guidelines, including:
  - What to do with TRST* signals
  - Buffering and layout of TAP IO signals
  - Care over the boundary-scan to non-boundary-scan interfaces
  - Setting up to program on-board Flash devices
  - Managing non-compliant devices
  - Mixed real-nail virtual-nail environments: maximising the use of physical nails in a flying probe/in-circuit test environment.

BOARD DFT GUIDELINES: XILINX VIRTEX-II PRO™ FPGA

- Introduction to the Virtex-II Pro FPGA
- 1149.1 JTAG characteristics
- 1532 characteristics
- Internal PPC405 block and design debug options
  - Linking the FPGA JTAG port to the PPC405 JTAG port
  - Board-level access to the PPC405 JTAG port
- DFT/Test guidelines
  - Configuration modes
  - Board-level access requirements
  - From the BSDL file
  - General FPGA test guidelines

BOUNDARY-SCAN TESTABILITY: HOW TO CONDUCT A DFT REVIEW

- Data requirements
- Chip-level checks: BS and NBS devices
- Board-level checks: multiple types
- Comprehensive review checklist
- Case study: a real example

TESTING HIGH-SPEED BUSES

- Parallel/serial high-speed buses
  - PCI-Express and other high-speed buses
  - SerDes design styles
  - DC- and AC-coupled LVDS interconnects
  - Bit Error Rates and "eye" diagrams
- Defects associated with LVDS interconnects
- Need for at-speed test
- Loopback test styles:
  - All in the chip (e.g. Intel® I-BIST)
  - All in the ATE channel card
  - Hybrid solution
- AC-coupled LVDS interconnects: limitations of 1149.1 and 1149.4
- IEEE 1149.6-2003 "AC-EXTEST" Standard
  - Modified TX boundary-scan cell
  - Modified RX test receiver
  - AC-PULSE and AC-TRAIN instructions
  - Combinations of DC and AC coupling
  - Changes to BSDL
  - Status of 1149.6

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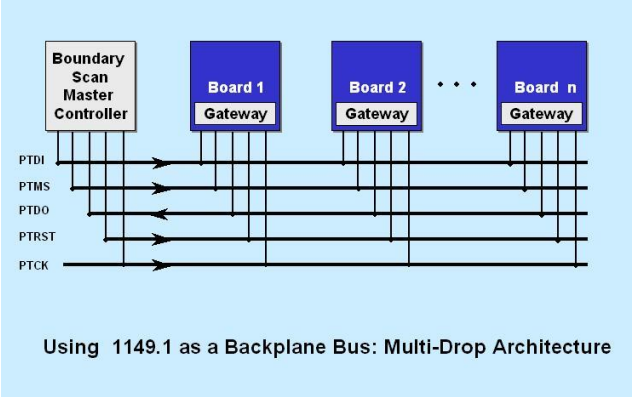
Day 3
Applications of Boundary Scan to System And Field-Service Test, Additional Board Test/DFT Topics, Quizzes



Using 1149.1 as a Backplane Bus: Multi-Drop Architecture

IEEE 1149.1 boundary scan was originally intended to solve board test interconnect problems on limited access boards. Boundary-scan technology now has a much-wider application to all manner of board and system test problems. Several companies supply boundary-scan support devices that allow 1149.1 to be used as a backplane test bus. This opens up possibilities of backplane interconnect test and multi-drop architectures, enabling backplane-to-board-to-chip diagnostics in system integration and field service scenarios. Day 3 discusses these applications and also includes a number of additional and in some cases specialised items. The extra topics include an introduction to the various styles of electrical board test (In-Circuit Test and its Manufacturing Defect Analyser and Flying Probe Test variants) and non-electrical board test (Automated Optical Inspection and Automated X-Ray Inspection). IEEE 1149.4, targeted at mixed-signal devices is also included, as is the increasingly important topic of IP security in an 1149.1-enabled device, the impact on board test of the move to lead-free solder, and creating BSDL files for System-in-Packages.

In addition, there are a variety of live quizzes on the various Standards

USING 1149.1 AS A SYSTEM-LEVEL BACKPLANE TEST BUS FOR MULTI-BOARD SYSTEMS

- Using 1149.1 as a backplane bus: ring, star and multi-drop architectures
- The need for special enabling devices: backplane test-bus-master controllers, addressable gateway devices, and test-program sequencers
- Principles of backplane board-to-board interconnect test
- Detection versus diagnostics: re-use of chip DFT structures (scan thru TAP, RUNBIST modes)
- Introduction to system-level eXternal Boundary Scan Test (XBST) and Embedded Boundary Scan Test (EBST)
- XBST and EBST use scenarios
- Case studies: Motorola Networks, BAE Systems

PLANNING FOR SYSTEM-LEVEL TEST

- Define system-level test objectives and requirements
- What type of tests?
- Test sources?
- Choosing a backplane test-bus protocol
- Test manager access: local or remote?
- Hierarchical multi-drop requirements?
- Fixing the Master-Slave architecture
- Selecting a scan-support chip set vendor
- Selecting a test manager support vendor
- Linking boundary scan with other test styles

STATUS OF THE System JTAG (SJTAG) INITIATIVE

- What it is
- What problem is being solved
- Initial focus on the micro and Advanced Telecommunications Architecture
- Status of SJTAG

PUTTING IT ALL TOGETHER

- Leveraging DFT techniques "above the chip" and "above the board": product life-cycle and economic view

FURTHER OPTIONAL TOPICS

BOARD TEST TECHNIQUES

- Electrical test: in-circuit test, functional test, manufacturing-defect analysers
- Driver/sensor pin electronics
- Non-electrical test: automated optical inspection, automated x-ray inspection
- ICT + AXI + AOI mix
- Emulation test: µProcessor, memory, bus-timing
- PXI "rack and stack"

IEEE 1149.4-1999 MIXED-SIGNAL TEST BUS STANDARD

- Architecture: Test Bus Interface Circuit, internal test buses, analog boundary modules, PROBE instruction
- Dot One mode and Analog mode

- National Semiconductor STA 400 Demonstrator device

IEEE 1149.1 NON-COMPLIANCE: CAUSE AND EFFECT (BSDL "HORROR STORIES")

- What is BSDL?
- Various versions of BSDL
- Examples of non-compliance: software and hardware horror stories
- Suggestions for improvement
- Checking BSDL

THE 2001 VERSION OF IEEE 1149.1: MAIN CHANGES

- Change to *EXTEST* opcode
- *SAMPLE/PRELOAD* separation
- New boundary-scan cells: BC_8 thru BC_10
- BSR/System logic sharing
- Bus KEEPERs
- Mandatory BSDL

TESTABILITY VERSUS SECURITY THRU 1149.1

- The big question: how easy …?
- Who do we worry about, and why?
- Access via 1149.1 and internal scan chains
- cPLDs and FPGAs
- Data requirements

TEST STRATEGIES FOR SYSTEMS-IN-PACKAGES

- Product complexity driving SiP packaging styles
- SiP test issues: One or more BSDL files?
- Philips SIP-TAP solution: BYPASS register(s), IDENT register(s), TRST*

MAJOR CHANGES IN COMPONENT AND PCB DESIGN AND MANUFACTURING TECHNIQUES AND THEIR IMPACT ON BOARD TEST

- Change to Pb-free solder
- Effect of Lower Supply Voltage Devices
- Increasing Miniaturization
- Gbit/s Data Transfer Rates
- Ever-Larger SoC/SiP Devices
- More Mixed-Signal Devices
- More Security on Board IP
- Increased Use of PCB Backpanels

LIVE MULTI-CHOICE QUIZZES

- IEEE 1149.1: chip and board
- IEEE 1149.4
- IEEE 1532

SOURCES OF FURTHER INFORMATION

Attendees will receive a copy of the presentation slides, including accompanying text.

COURSE PRESENTER

Eric Cormack is an independent consultant in Design-For-Test (DFT), Design-for-Manufacture(DfM) and Design-for-Debug(DfD) consulting in product life-cycle DFT strategies, and delivering on-site and open educational courses in DFT technologies.

Previously, he has worked for **Ferranti Computer Systems**, **Testech**, **General Hybrid**, **GenRad, Hitachi Micro Systems Europe and Philips/NXP Semiconductors**. Between 1981 and 1986, he was a test solutions consultant for Testech in the USA establishing offices on East and West coasts. During this time, he was responsible for providing DfT training and consultancy for both commercial and military companies. He then came back to the UK and worked with GenRad as a tools developer and trainer, established a DfT group in Hitachi Micro Systems Europe and provided DfT, DfM and DfD solutions to complex SoC DVB devices for TV/Video applications within Philips/NXP Semiconductors.

He is a core-group member of **SJTAG.**

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