Techniques for Designing Testable ICs: Internal Scan, BIST, Boundary Scan and SOC Techniques

Presented by Eric Cormack, DFT Consultant

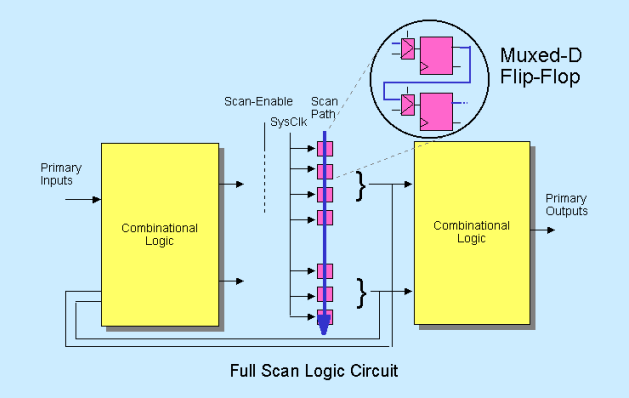
DURATION: 3 days

TARGET AUDIENCE digital chip designers and test engineers, test-synthesis tool developers and product support engineers.

MOTIVATION OBJECTIVES: to motivate chip designers to consider life-cycle test needs as an integral part of a product design process to the point where they proactively design in testability.

TEACHING OBJECTIVES: determine the fundamental limits of test technology and hence identify the "why" of DFT; teach the "how" of DFT solutions - internal scan, Built-In Self Test, 1149.1 boundary scan and associated 1149.4 mixed-signal test bus and 1149.6 "AC-EXTEST" Standards; show application to System-on-Chip and System-in-Package devices.

Day 1
Basics of Design For Test (Refresher), Internal Scan Design



Day 1 is a general introduction to the notional concepts of Design-For-Test and its relationship with device life-cycle test and overall quality requirements. The day starts with a refresher on the basics of DFT covering the classic fault models (stuck-ats, bridging and propagation delay) and their relevance to modern-day silicon defects. This is followed by a brief introduction to I_{DDQ} current test. But the bulk of the day is devoted to the DFT technique of internal scan: where it came from, what it is, and an in-depth look at the practical issues based on using commercial tools.

DFT BASICS: REFRESHER
- DFT, quality and test
- IC defects and fault models
- I_{DDQ} Testing
- Chip ATE

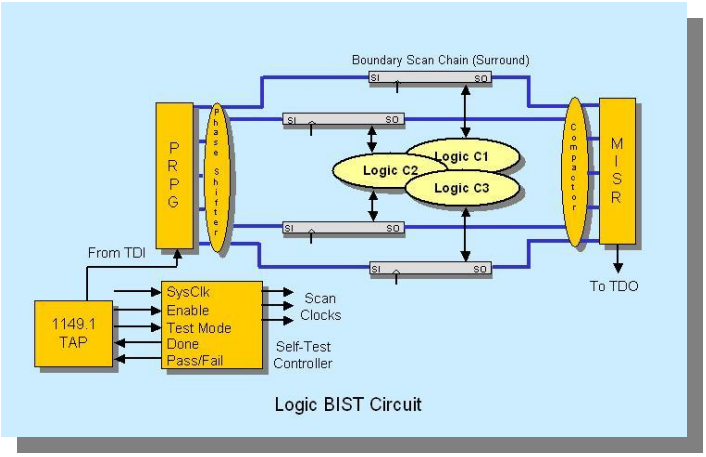
INTERNAL SCAN DESIGN: BASICS
- ATPG: sensitive path concepts (combinational and sequential application)
- Assessing fault coverage: fault simulation
- Reasons for and principles of scan design
- Edge-Sensitive Scan Design: MDFF
- Multi-cycle paths and false paths
- PLD design example

INTERNAL SCAN DESIGN: SCAN SYNTHESIS
- Rule checking: identifying candidate flip-flops for scan chain insertion
- Scan-chain balancing (partitioning)
- Single or multiple clock in scan mode?
- Module-to-module scan chain linking
- Multi-cycle paths and false paths
- Flip-flop ordering/reordering in scan chains
- Handling embedded memory: wrapper, bypass and write-through techniques
- Scan chain insertion
- Adding disabling logic to avoid contention during scan-in/scan-out operation
- Designer responsibilities

Day 2
DFT Rule Checking, Detection of Delay Faults, Built-In Self Test, Test Data Compression

Day 2 continues with some of the more recent developments in internal scan and then concentrates on Built-In Self Test, looking at the two main industrially-accepted Built-In Self Test techniques of memory BIST (for multiple instances of embedded memory) and logic BIST (as a natural extension of full scan circuits). The logic BIST presentation is preceded by a discussion of basic building blocks (LFSRs, MISRS)

The day concludes with a discussion of the recent test-data compression techniques, and how they stack up against logic BIST.



Logic BIST Circuit

DFT GUIDELINES FOR ASICs

- Asynchronous Rules
- Clock Rules
- Latch Rules
- Memory BIST Rules
- Scan Chain Rules
- Topology Rules
- RAM Rules
- Logic BIST Rules
- Testability Analysis
- Tristate Rules

DFT RULE-CHECKING AT THE RTL

- RTL DFT Rule Checkers – what are they?
- Tool flow and rule checks

AT-SPEED TESTS THRU SCAN CHAINS

- Path delay and transition delay faults
- What causes delay faults?
- How are they modelled?
- Pattern generation techniques
- Pattern application techniques (through scan chains)
- Launch-on-Shift and Launch-on-Capture scan chain protocols

DIAGNOSING FAULTS THRU SCAN CHAINS

- Using scan chain results
- Back coning (path tracing) techniques
- Creating and using a fault dictionary
- DFT/Test aids to accurate diagnosis

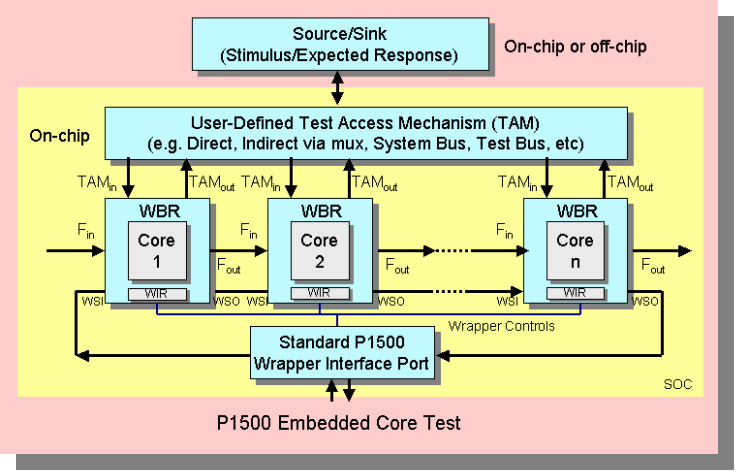
BUILT-IN SELF TEST (BIST)

- Elements of a BIST circuit
- Motivation for and potential benefits of BIST
- RAMs: failure mechanisms and Marching algorithms (6N, 9N, March C-, ….)
- BIST at the device level: memory BIST (SRAM, DRAM, ROM)
- BIST architecture for multiple instances of embedded memory
- BIST for scan design ICs (logic BIST)
- Use of pseudo-random pattern generation and data compaction techniques: pseudo-random properties, aliasing
- Building blocks: Linear Feedback Shift Register (LFSR) and Multiple-Input Signature Register (MISR)
- Logic BIST architecture
- At-speed testing thru logic BIST
- Overcoming pseudo-random resistance: test-point insertion, re-seeding, bit flipping
- Scan-thru-TAP mode

TEST DATA COMPRESSION TECHNIQUES

- What is test data compression?
- Test data compression/decompression techniques: EXOR, Mux, LFSR re-seeding
- Test response compaction techniques: EXOR, MISR
- Handling X states
- Logic BIST versus test data compression

Day 3
Boundary Scan (1149.1) And Its Application To Designing Testable System-On-Chip Devices (1500), IJTAG, DFT Testers



The IEEE 1149.1 Boundary-Scan Standard was developed originally to solve board interconnect test problems but boundary-scan features are inserted into the devices by device designers. Day 3 focuses first on the chip-level architecture of 1149.1 so that device designers (a) know what they have to do during design and (b) know why they are asked to insert the boundary-scan logic. Later in the day, attention turns to the issues of designing testable System-On-Chip devices. Parallels are drawn between testing devices and interconnects on boards, and testing cores and their interconnects on SOC devices. Boundary-scan technology can be used to solve the SOC test issues but the current solutions do not use "pure" 1149.1. The IEEE 1500 Embedded Core Test Standard is presented The day concludes with a discussion of the recent IEEE P1687 (IJTAG) initiative and the emergence of the PC-based low-cost chip DFT testers.

IEEE 1149.1-2001 BOUNDARY-SCAN STANDARD: CHIP LEVEL ONLY

- Motivation for boundary scan: use of surface mount packaging, double-sided multi-layer boards
- Device-level architecture: Test Access Port (TAP) controller, instruction register, bypass register, identification register, boundary-scan register, access to internal registers
- Mandatory and optional public instructions: BYPASS, EXTEST, PRELOAD, SAMPLE, INTEST, IDCODE, USERCODE, CLAMP, HIGHZ, RUNBIST
- Forms of boundary-scan cells: BC_1 to BC_10
- Use at board level (overview only)
- Languages and format: Boundary-Scan Description Language (BSDL)

IEEE 1149.4-1999 MIXED-SIGNAL TEST BUS STANDARD (OPTIONAL)

- Architecture: Test Bus Interface Circuit, internal test buses, analog boundary modules, PROBE instruction
- Dot One and Analog modes
- National Semiconductor's STA400 demonstrator device

IEEE 1500 STANDARD: TEST STRATEGIES FOR SYSTEMS-ON-CHIPS

- SOC definition, embedded cores, test problems
- 1500 Embedded Core Test Standard: concepts
- Wrapper Boundary Registers, Instruction Register and control signals, Bypass Register, wrapper modes, serial and parallel ports, wrapper cells, instruction set
- Example of a 1500-wrapped core
- IEEE 1450.6 Core Test Language
- Relationship of IEEE 1500 with IEEE 1149.1

TEST STRATEGIES FOR SYSTEMS-IN-PACKAGES

- Product complexity driving SiP packaging styles
- SiP test issues: One or more BSDL files?
- Philips SIP-TAP solution: BYPASS register(s), IDENT register(s), TRST*

IEEE P1687 (IJTAG) DRAFT STANDARD FOR ACCESS AND CONTROL OF INSTRUMENTATION EMBEDDED WITHIN A SEMICONDUCTOR DEVICE

- Background: use of 1149.1 Test Access Port to access embedded instruments
- IEEE P1687 (IJTAG) evolution, scope, motivation, problem statement
- Evolution of embedded instrumentation – revisited
- Hardware interface proposal: current status
- Conclusions, issues, getting involved

DFT TESTERS

- The emergence of the low-cost PC-based chip DFT tester

DFT CONCLUSIONS

- Leveraging DFT techniques "above the chip" and "above the board": product life-cycle view

FURTHER OPTIONAL TOPICS

TESTING HIGH-SPEED BUSES

- Parallel/serial high-speed buses
  - PCI-Express and other high-speed buses
  - SerDes design styles
  - DC- and AC-coupled Low-Voltage Differential Signal (LVDS) interconnects
  - Bit Error Rates and "eye" diagrams
- Defects associated with LVDS interconnects
- Need for at-speed test
- Loopback test styles:
  - all in the chip (e.g. Intel® I-BIST)
  - all in the ATE channel card
  - hybrid solution
  - Potential application to the Mobile Display Digital Interface (MDDI)
- AC-coupled LVDS interconnects: limitations of 1149.1 and 1149.4
- IEEE 1149.6-2003 "AC-EXTEST" Standard
  - Modified TX boundary-scan cell
  - Modified RX test receiver
  - AC-PULSE and AC-TRAIN instructions
  - Combinations of DC and AC coupling
  - Changes to BSDL
  - Status of 1149.6

EMULATION (IEEE 5001 NEXUS STANDARD)

- Microprocessor core emulation requirements
- Use of 1149.1 TAP and the need for a high-speed port
- Nexus recommended registers
- Nexus compliance classes 1 thru 4
- Status of the Nexus Standard

IEEE P1581 *STATIC COMPONENT INTERCONNECTION TEST PROTOCOL AND ARCHITECTURE* STANDARD

- What problem are we solving?
- P1581 concept
- Transparent Test Mode
- Comment on DFT guidelines
- P1581 status, who's who, and conclusions

IEEE P1149.7 *REDUCED-PIN AND ENHANCED-FUNCTIONALITY TEST ACCESS PORT AND BOUNDARY-SCAN ARCHITECTURE.* "CJTAG"

- Origins of cJTAG
- What problem is solved?
- Processor emulation requirements
- The cJTAG problem definition, and solution
- 4 wires down to 2 wires
- Emulation scenarios
- Advanced test access port: use of Zero-Bit Shift sequences
- cJTAG at the board level
- Status of cJTAG

SOURCES OF FURTHER INFORMATION

Attendees will receive a copy of the presentation slides, including accompanying text.

COURSE PRESENTER

Eric Cormack is an independent consultant in Design-For-Test (DFT), Design-for-Manufacture(DfM) and Design-for-Debug(DfD) consulting in product life-cycle DFT strategies, and delivering on-site and open educational courses in DFT technologies.

Previously, he has worked for **Ferranti Computer Systems**, **Testech**, **General Hybrid**, **GenRad, Hitachi Micro Systems Europe and Philips/NXP Semiconductors**. Between 1981 and 1986, he was a test solutions consultant for Testech in the USA establishing offices on East and West coasts. During this time, he was responsible for providing DfT training and consultancy for both commercial and military companies. He then came back to the UK and worked with GenRad as a tools developer and trainer, established a DfT group in Hitachi Micro Systems Europe and provided DfT, DfM and DfD solutions to complex SoC DVB devices for TV/Video applications within Philips/NXP Semiconductors.

He is a core-group member of **SJTAG**.

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